Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

B.E/B.TECH DEGREE END SEMESTER THEORY EXAMINATIONS, NOV/DEC 2025

Third Semester

Electronics and Communication Engineering

EC3352- Digital Systems Design

Regulations - 2021

Duration : 3 Hrs *Maximum : 100 Marks*

*PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)*

Q.No	*Questions*	*BTL*	*CO*	*Marks*
1.	State two Boolean algebra theorems used for simplification.	L1	1	2
2.	Identify the type of Boolean function represented by a Karnaugh map with all cells filled.	L2	1	2
3.	Name the circuit used to convert binary to BCD code.	L1	2	2
4.	Determine the output of a 4-to-1 multiplexer when all select lines are 0.	L2	2	2
5.	List two types of triggering used in flip-flops.	L1	3	2
6.	Identify the type of counter which circulates a single high bit.	L2	3	2
7.	Define a stable state in asynchronous circuits.	L1	4	2
8.	Recognize the type of hazard that occurs due to essential changes in input only.	L2	4	2
9.	State two logic families with high noise immunity.	L1	5	2
10.	Identify the programmable device used to implement a fixed combinational logic function.	L2	5	2

*PART – B (ANSWER ALL QUESTIONS) (Marks 5*16 = 80)*

Q.No		*Questions*	*BLT*	*CO*	*Marks*
11.	a	Simplify the following expressions using Boolean Postulates and theorems: (i) F1 = (AB)'(A' + B)(B' + B): (ii) F2 =(A + C)(AD + AD') + AC + C: (iii) F3 = A'(A + B) + (B + AA)(A + B') (iv) F4 = xy + x(wz + wz')	L3	1	16
		Or			
	b	Simplify the following Boolean expression using Quine McCluskey method and determine the Prime Implicants and Essential Prime Implicants: F= ∑m(1,2,3,9,12,13,14,15) + ∑d(0,4,7,10,11). Draw the logic diagram using NAND gates only.	L3	1	16
12.	a	Design a 4-bit binary parallel adder to add two numbers A = 1011 and B = 1101. Show all intermediate carry values and the final sum.	L3	2	16
		Or			
	b	Design a 3-to-8 decoder circuit for inputs X, Y, Z. List all output states for all possible input combinations and draw the logic diagram.	L3	2	16

13.	a	A JK flip-flop has J = A + B, K = $A \cdot \overline{B}$, and initial state $Q_0 = 0$. Draw the timing diagram for inputs A and B given below for four clock pulses: • A = 0, 1, 0, 1 • B = 1, 0, 1, 0	L3	3	16
		Or			
	b	Design a 4-bit synchronous up/down counter using T flip-flops. Derive the excitation table, the flip-flop input equations, and show the state transition diagram for counting up and down.	L3	3	16
14.	a	Define races and its types. Explain race free binary assignment for designing asynchronous sequential circuit.	L4	4	16
		Or			
	b	Analyze a given asynchronous circuit and identify all static, dynamic, and essential hazards. Propose modifications to eliminate the hazards and draw the updated circuit.	L4	4	16
15.	a	Compare the characteristics of TTL, CMOS, and ECL logic families in terms of propagation delay, fan-in, fan-out, and noise margin.	L3	5	16
		Or			
	b	Design a combinational logic circuit using PLA to implement a given Boolean function and discuss its advantages over standard IC implementation: $F_1 = \sum m(1,3,5,6,7)$; $F_2 = \sum m(0,2,4,6)$	L3	5	16